Hindawi Publishing Corporation
Advances in OptoElectronics
Volume 2011, Article ID 627802, 15 pages
doi:10.1155/2011/627802

Review Article

Reconfigurable Integrated Optoelectronics

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Received 26 November 2010; Accepted 2 March 2011

Academic Editor: Lucimara Roman

Integrated optics today is based upon chips of Si and InP. The future of this chip industry is probably contained in the thrust towards optoelectronic integrated circuits (OEICs) and photonic integrated circuits (PICs) manufactured in a high-volume foundry. We believe that reconfigurable OEICs and PICs, known as ROEICs and RPICs, constitute the ultimate embodiment of integrated photonics. This paper shows that any ROEIC-on-a-chip can be decomposed into photonic modules, some of them fixed and some of them changeable in function. Reconfiguration is provided by electrical control signals to the electro-optical building blocks. We illustrate these modules in detail and discuss 3D ROEIC chips for the highest-performance signal processing. We present examples of our module theory for RPIC optical lattice filters already constructed, and we propose new ROEICs for directed optical logic, large-scale matrix switching, and 2D beamsteering of a phased-array microwave antenna. In general, large-scale-integrated ROEICs will enable significant applications in computing, quantum computing, communications, learning, imaging, telepresence, sensing, RF/microwave photonics, information storage, cryptography, and data mining.

1. Introduction

This paper focuses on reconfigurable chips and boards that can interface with free-space light beams and optical fibers. The stacked, layered 3D chip is an important new trend discussed here. One goal of this paper is to present a building-block theory of reconfigurables in which a system is formed by interconnecting fixed and changeable modules, each of which has a distinct function. Those functions are identified, and several examples of theory are given. Some examples pertain to chips already built; others are proposals for future chips. Over the next five years, the main optoelectronics research challenge is the large-scale integration (LSI) of low-energy reconfigurable photonics in a cost-effective manner. Our theory provides a framework for innovative R&D in LSI but does not answer basic questions about the function and architecture of new LSI chips. Readers of this paper are called upon to answer those questions.

The semiconductor chip or substrate assumed in this paper is typically silicon or indium phosphide, but we will be agnostic about which materials system should be used. The wavelength of operation would be in the visible-through-mid-infrared [3], typically in the 1550 nm telecom/datacom wavelength band. Opto-electronics (OE) refers to a marriage of optics with electronics, whereas electro-optics (EO) signifies an optical device that is controlled or actuated by an electrical signal. The term integrated circuit (IC), well known in electronics, signifies here an onchip network of waveguided components. This paper considers active photonic integrated circuits (PICs) and opto-electronic integrated circuits (OEICs), in particular reconfigurable PICs or RPICs and reconfigurable OEICs or ROEICs. The term active refers to EO devices such as lasers, amplifiers, photodetectors, modulators, and switches.

2. System on a Chip and System on a Board

Figure 1(a) shows the top view of the ROEIC chip comprised of the RPIC (nanophotonics) and the nanoelectronics. In practice, most chips, whether ROEIC or not, will be bonded to a mother board. Figure 1(b) illustrates the most general case of this motherboard which includes nanoelectronic chips and monolithic microwave integrated circuits (MMICs) as well as RPIC, PIC, ROEIC and OEIC chips. Applications include digital and analog photonics along with RF photonics.

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
NOV 2010		**00-00-2010 to 00-00-2010**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Reconfigurable Integrated Optoelectronics	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Air Force Research Laboratory,Sensors Directorate,Hanscom AFB,MA,01731**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**15**	

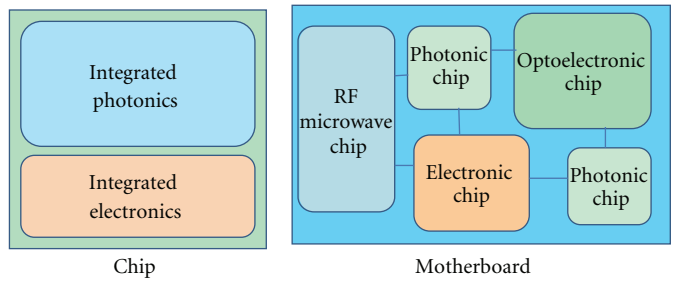


Figure 1: Top view of (a) optoelectronic system on a chip, (b) opto-electro-microwave system on a board.

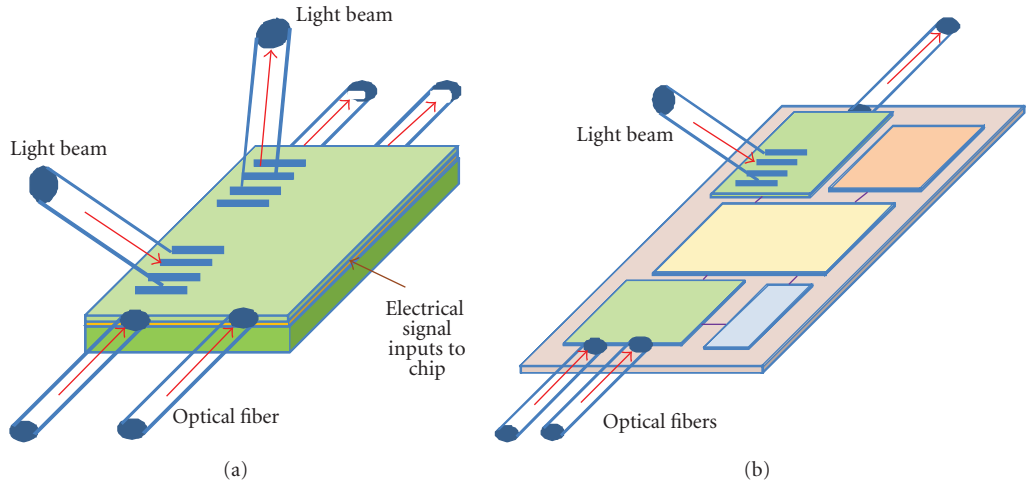


Figure 2: The external optical interfaces of (a) the chip and (b) the board.

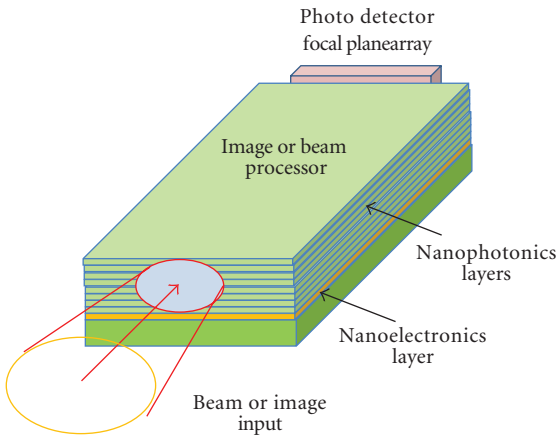


Figure 3: Optical beam processing and image processing in a 3D multilayer RPIC chip.

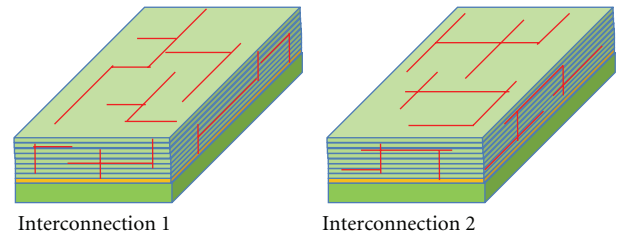


Figure 4: Waveguided optical signal processing in 3D by reconfiguring the in-chip 3D networks.

The ROEIC shown in Figure 1(a) is a very capable but "futuristic" chip that contains seamless OE integration. The intent is to manufacture this chip in a high-volume semiconductor foundry. This is an important goal of the photonics industry; however, few chips like these are available today because of the considerable development costs required to create them. With the advent of multiuser OE foundries and photonic-component "libraries", this cost barrier will come down and ROEICs will then "blossom". But in the meantime, the "easy" approach is to place the RPIC and its companion nanoelectronics on different chips as shown in Figure 1(b). The Figure 1(a) chip is likely to have a photonic layer integrated upon an electronics layer with "through-photonic vias" for electrical communication to EO components.

3. Optical Interfaces for Chip and Board

Now we consider how chips and boards are coupled to the external world. These optical interfaces are shown in

Figures 2(a) and 2(b) for chip and board, respectively. Glass and polymetric fibers can be end-coupled to the optical chips, or even surface coupled. In addition, light beams traveling in free space can launch into and exit from chip waveguides via surface gratings as shown. Light sources can be external too. Of course, many laser diodes can be integrated onchip in the RPIC, but a popular new approach is to utilize an off chip "optical power supply" consisting of laser light sent into the chip via an optical fiber or fibers. Of particular value is the multiwavelength optical source, a series of distinct spectral lines coming in from a comb laser by means of fiber.

4. The 3D Chip

Thanks to R&D projects sponsored by government and industry, electronics specialists are becoming familiar with the significant potential of 3D electronic chips. We are suggesting here that 3D opto-electronic chips have even greater promise. This OE approach has already received coverage in our proposal of 3D plasmo-photonic chips [12] and in the experimental 3D photonic work of the MIT team on the DARPA EPIC program where two photonic layers and one electronic layer were employed. However, the story of 3D ROEIC approaches-and-applications is just beginning. The idea is that the properly designed 3D ROEIC chip will be more "competent" than any 2D ROEIC. We envision the 3D ROEIC as comprising N layers of RPICs sitting on top of one electronics layer.

There are two ways in which to construct the 3D stack: layer-by-layer epitaxial growth, and the stacking and bonding of semiconductor nanomembranes recently demonstrated by three teams on the AFOSR multiuniversity research initiative (MURI). The 3D RPIC region can consist of a 3D photonic crystal such as the stacked rod-and-hole membranes shown by the MIT team [2] on the above MURI, or a vertical ensemble of 2D electrooptical waveguiding layers. We identify two types of 3D chip functioning: processing of optical beams-and-images and waveguided optical signal processing. These are illustrated in Figures 3 and 4.

In Figure 3, the input and output ends of the stack are polished for optical access. The processing in Figure 3 is a new approach to "volumetric optical processing"—a layered semiconductor volume approach in which the stack height is often limited to about ten wavelengths. Traditionally, optical processing in a "volume of space" is a free-space approach employing lenses and spatial light modulators (SLMs). By contrast, an image in Figure 3 is processed as a set of "image slices" in layered semiconductor space. To attain optical correlation (for example) would require slab waveguides, an ensemble of unique slab lenses for Fourier transformation, and a row-by-row SLM. Alternatively, beam processing in Figure 3 could consist of (1) optical beamsteering or (2) phase-matched 2nd order or 3rd order nonlinear optical processing of a beam whose waist equals the stack height, or (3) spectroscopy in 3D in which a spectrally broad light source impinges on the chip and is layer-by-layer wavelength demultiplexed for determining the absorption spectrum of an onchip sample.

The steering approach for Figure 3 has received validation by experiments at the University of Texas at Austin illustrated schematically in Figure 5. That MURI team used two bonded photonic layers containing phase shifters and time delays to steer on optical beam in one dimension [1].

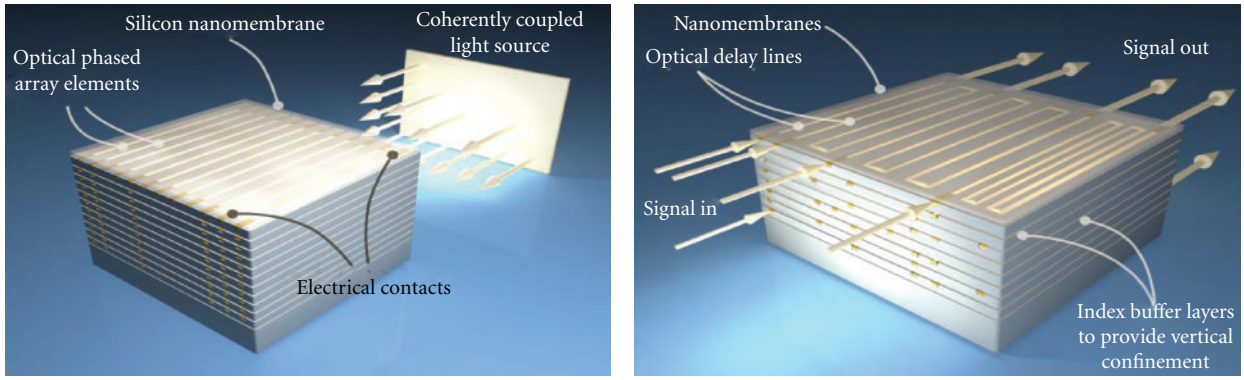
The "ultra waveguided processing" of Figure 4 employs changeable 3D optical networks within the stack. In this 3D routing and rerouting, the vertical interlayer optical connections will require invention, and there are challenges to be met in making electrical vias between layers and heat-conduction regions within the stack. The light sources in Figure 4 could be onchip or brought in by a fiber ribbon (not shown). The 3D photonic crystal [2] of Figure 6 offers one path to Figure 4; dielectric layering gives another.

5. Building-Block Theory

A configuration is a state of a system in which the system performs a specific function. Reconfiguration is a change in that function, often a mild or moderate change within the same application area. The system is programmed by commands that are usually electrical signals, although this state-changing could be done also using thermo-optical, mechano-optical, magneto-optical or opto-optical inputs. The speed of reconfiguration can be fast or slow, depending upon need. The basic tenant of our theory is that any system can be *decomposed* into building blocks or modules; some modules are fixed, others changeable. Conversely, any system is *composed* of modules. Modules are interconnected both optically and electrically. With these definitions, let's move forward to see how reconfiguration works. First let's examine the input/output (I/O) connections of optical (O/O′) and electrical (E/E′) signals to the ROEIC. The nine possibilities are shown in Figure 7.

Any ROEIC system is composed of subsystems, each of which is a collection of connected fixed- and-variable modules as shown in Figure 8. Therefore, it is clear that the system can be reconfigured by reconfiguring the subsystems and/or their interconnections (optical and/or electrical connects). We can see this by looking at the examples in Figures 9 and 10. Figure 9(a) illustrates a change in the interconnections, while Figure 9(b) shows a change in subsystems (identical "cells" in that case). Figure 10 shows in detail how the interconnect modifications of Figure 9(a) would be implemented by two onchip $N \times N$ EO matrix switches.

Generally, Figure 9(b) is more difficult to implement than Figure 9(a) because the Figure 9(b) designer must invent a way to change the subsystem function, whereas the Figure 9(b) "altered pathway" approach relies upon known optical switching practice. Figure 9(a) introduces the ideas of redundancy and diversity. For example, if a subsystem known as B in Figure 9(a) is a redundant backup for the subsystem known as A, then if A fails, the new connection of B will allow normal system functioning. If we purposely choose the subsystems in Figure 9(a) so that each one offers a rather different computation function, then we can easily



(a) (b)

Figure 5: Stacked-membrane 3D chip for photonic beam steering, courtesy of Hosseini et al. [1].

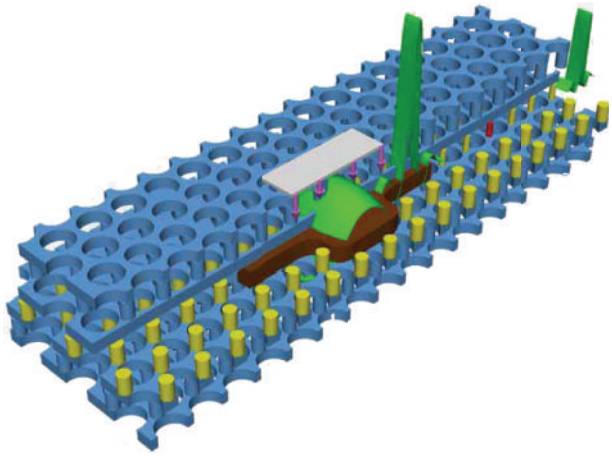


Figure 6: 3D photonic crystal for possible 3D reconfiguration, courtesy of Minghao Qi [2].

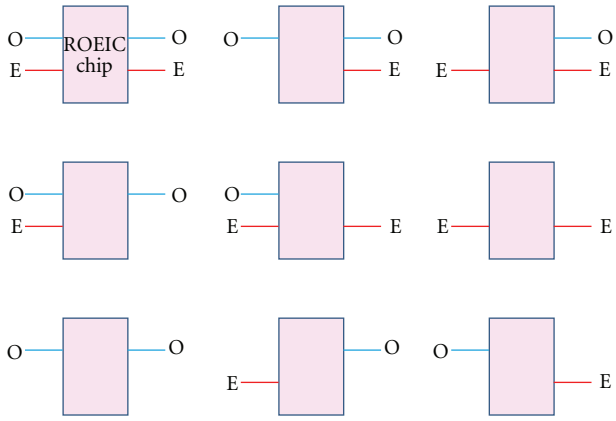


Figure 7: The useful optical and electric input/output to the ROEIC.

create a multiple-task computer by selecting one subsystem-at-a-time via the interconnects. Regarding the electrical programming of the subsystems, there are two possibilities illustrated in Figure 11; the groomed electrical signals are applied externally or they come from an onchip electronic circuit.

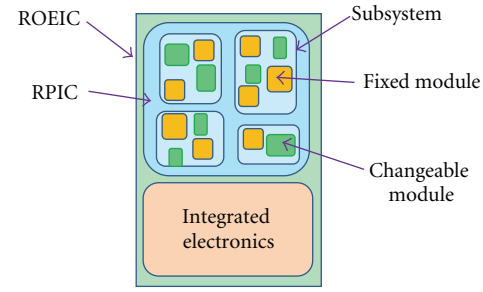


Figure 8: Subsystems are comprised of fixed and dynamic modules.

6. Fixed or Passive Modules

The first type of photonic module has an optical function that never changes. Taking into account the wavelength, amplitude, phase, polarization, linewidth, direction and velocity of optical waves, we have identified the principle types of passive modules as shown in Figures 12, 13, and 14. These include the "classical" linear optical functions as well as nonlinear optical functions—the latter employing either second-order or third-order nonlinearity for 3- or 4-wave mixing, respectively [13]. The NLO functions include sum- or-difference-frequency generation, parametric amplification, parametric oscillation, third harmonic generation, Raman amplification, wavelength conversion, supercontinuum generation, time-division demultiplexing, and time-to-frequency conversion. The linear and nonlinear functions take place in channel-waveguided devices. If we broaden the scope to include slab waveguiding, then we should include the linear photonic module functions of slab-beam focusing, deflection and spatial dispersion (e.g., via an echelle grating).

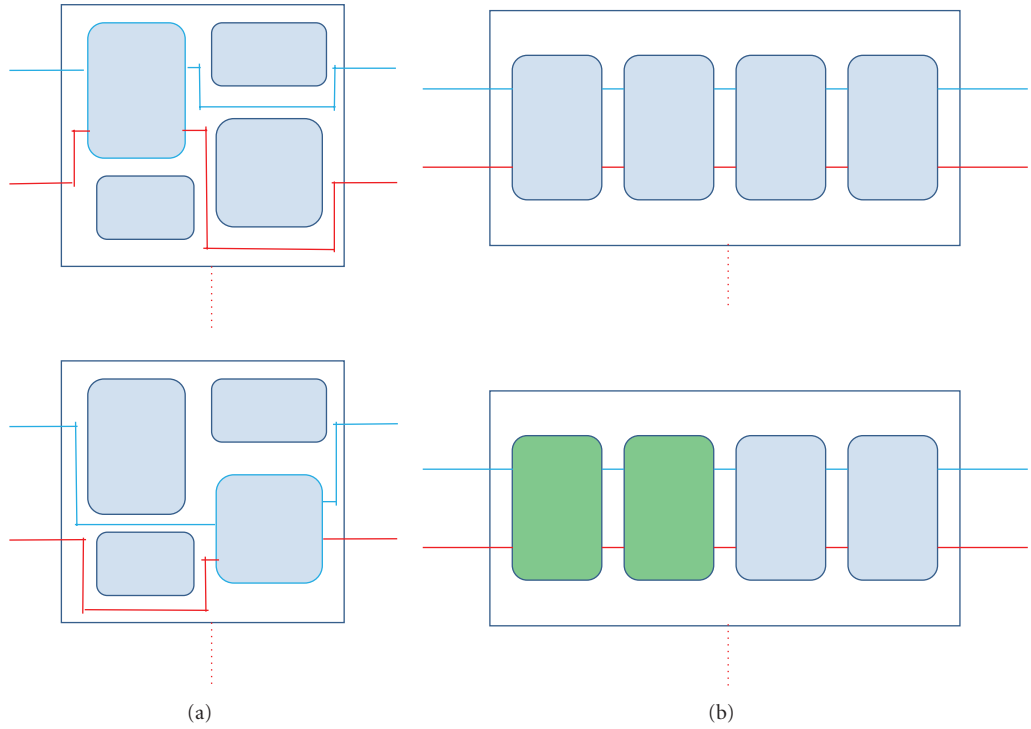


Figure 9: Chip reconfiguration by (a) altering the interconnections of subsystem modules and (b) altering the modules themselves.

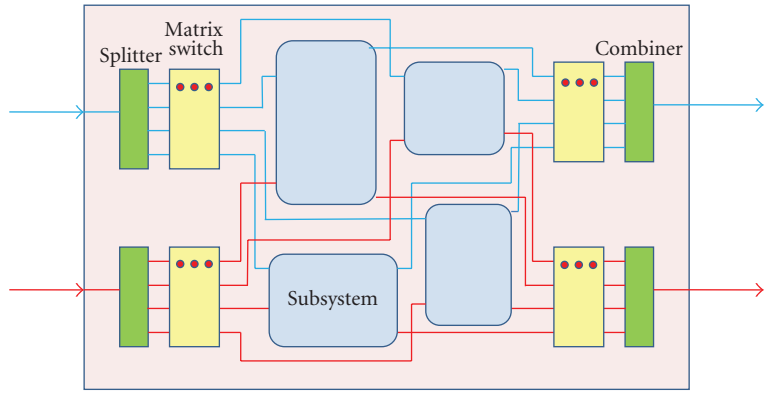


Figure 10: A technique for onchip EO reconfiguration of optical and electrical interconnections.

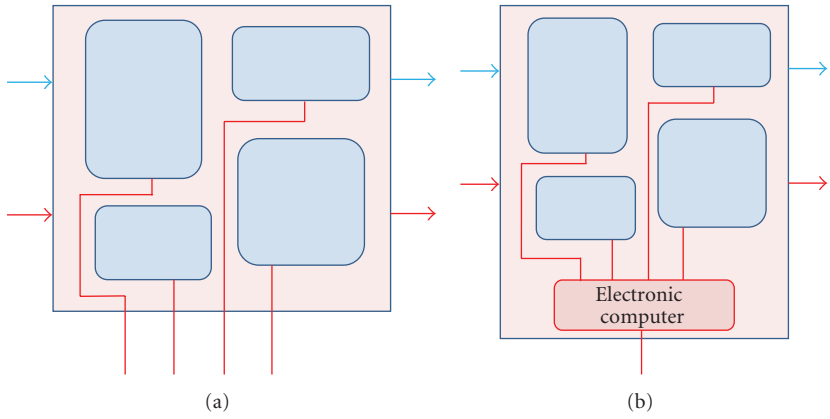


Figure 11: EO reconfiguration of the RPIC is accomplished by (a) externally applied signals or (b) signals from an onchip IC.

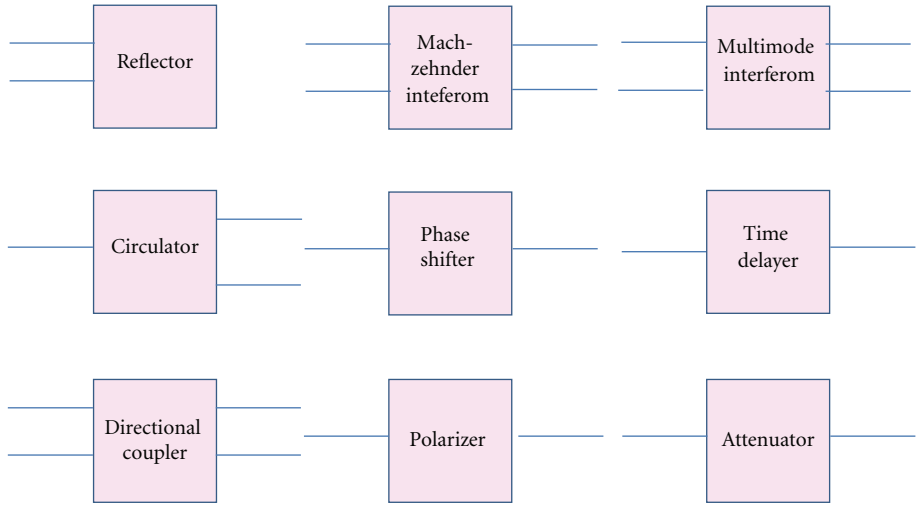


Figure 12: Passive photonic building blocks. The optical function has been labeled.

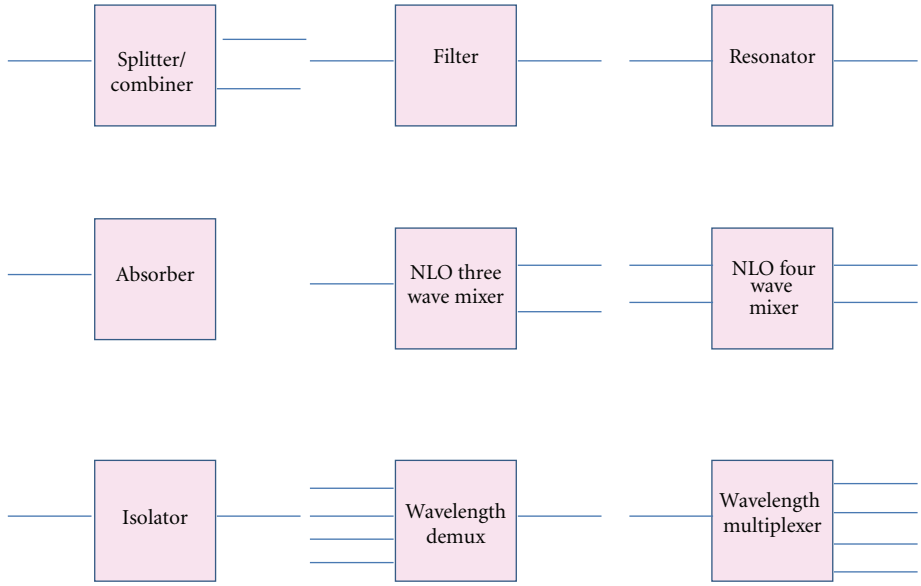


Figure 13: More fixed modules.

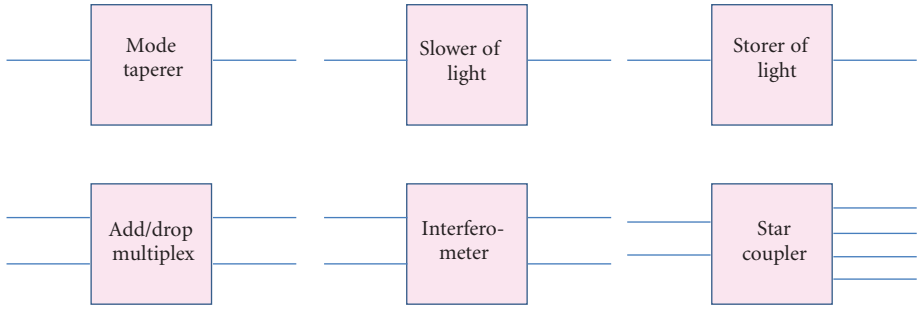


Figure 14: Additional passive blocks.

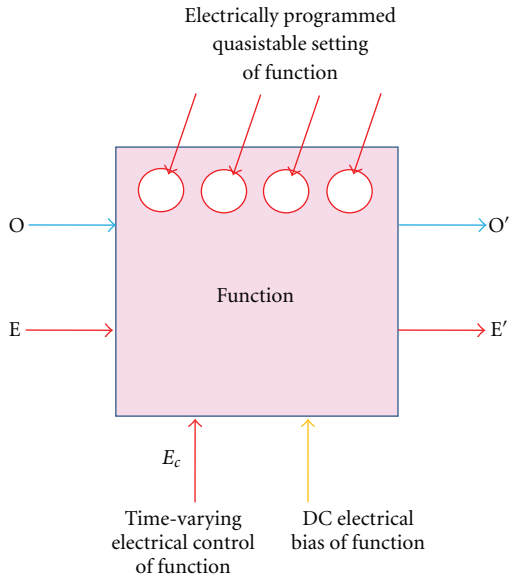


Figure 15: Generic diagram of a dynamic, programmed electro-optical building block.

7. Active Dynamic Modules

By means of electrical control signals applied to a module, the photonic function may be modified, giving reconfiguration. The applied signal may be rapidly varying in time, in either a digital or analog fashion. We call this "dynamic" reconfiguration. Alternatively the applied control signal could have a slow or quasistable time profile, producing a step change in configuration. We call that "programmed" reconfiguration. "Dynamic" refers to a continuous change; "programmed" is stably multivalued. We might say that dynamic is "programming on the fly". These possibilities are illustrated in Figure 15 where we show a set of symbolic programming "buttons" or settings. Quasi-stable inputs, often in the form of an electrical "1" or "0" are applied to each red circle. Dynamic input signals are shown by the bottom left red arrow. Usually, these active devices require some sort of electrical bias or power to operate, as indicated by the orange arrow at the bottom right. We will not address in this paper software issues such as programming a large-scale optical gate array to compile a library of system functions.

Our proposed library of reconfigurable building blocks is presented in Figures 16–18. We begin in Figure 16 with the modules suited for reconfiguring optical circuits—such as spatial routers, add-drop multiplexers and waveguided "shutters". Figures 17 and 18 present blocks for active tasks like the generation, detection, and modulation of light. The transducer shown is a sensor that transforms a physical or chemical variable into an optical response. Note that a few of the modules in Sections 6 and 7 can be subdivided into other modules: for example, the amplitude modulator could be resonant or nonresonant, and the directional coupler could be a 3 dB or 10 dB device.

Although magneto-optical devices have not been considered in Figures 16–18, those devices have the advantage of exhibiting stable states. Regarding the states of EO blocks in Figures 16–18, stability may come at a price. A stable EO state exists at zero control voltage, however a holding voltage will probably be required to maintain the "on" state over long periods. In addition to photonic modules shown in Figures 12–14 and 16–18, we believe that there is a set of plasmonic modules that can interface with photonics. Hence, there is a basis for reconfigurable nano-plasmo-photonics.

We will end this section with a few comments on the "all-optical" idea. Modules can be all-optical; however, we doubt that a system will be entirely optical because information enters and exits the system electrically. We have identified three AO reconfigurables: (1) a 3-wave or 4-wave "mixer" having one wave as the reconfiguration input, (2) a resonant optical modulator that relies upon a shift in a resonant mode induced by short-wavelength light, (3) the bistable III–V microdisk laser developed by scientists in Belgium [14, 15]; a waveguidecoupled emitter with stable states in its clockwise and counterclockwise modes. The LD is reconfigured by a light pulse that triggers either clockwise or counterclockwise emission.

8. The Challenges of Large-Scale OE Integration

The unique capabilities of integrated photonics will be fully realized by large-scale OE integration on a chip. LSI derived from high-volume manufacturing in a foundry will, we believe, offer low-cost, low-energy chips possessing revolutionary system-onchip capabilities. In other words, LSI is expected to give savings in cost-size-weight-power—plus superiority to existing optical systems due to new functionality related to high complexity and onchip electronics. LSI will become an excellent trajectory for the chip industry when LSI markets are identified. Our theory has created a "competent toolkit" for LSI. We have tried to provide a framework for enabling LSI with our library of modules for sophisticated ROEICs.

However, having the toolkit in hand does not satisfy all the LSI challenges. To illuminate that point, let us imagine that LSI is here today—imagine that we are given a chip that contains 10,000 nanophotonic components of our choosing. Then two questions arise immediately: (1) What is the specific function of the chip-system? (2) What is the specific architecture that will be employed to actualize the system? These are the fundamental issues of reconfigurable photonics going forward. Unfortunately the theory does not answer these questions. We need to add insight to theory, to add imagination about LSI functions and applications. And when we consider the architecture question, we may have to ask whether new EO components must be invented to satisfy that structure.

Let's answer the system question in a generic way. We estimate that future LSI will advance computing, quantum computing, communications, learning, telepresence, imaging, sensing, medicine, information storage, cryptography,

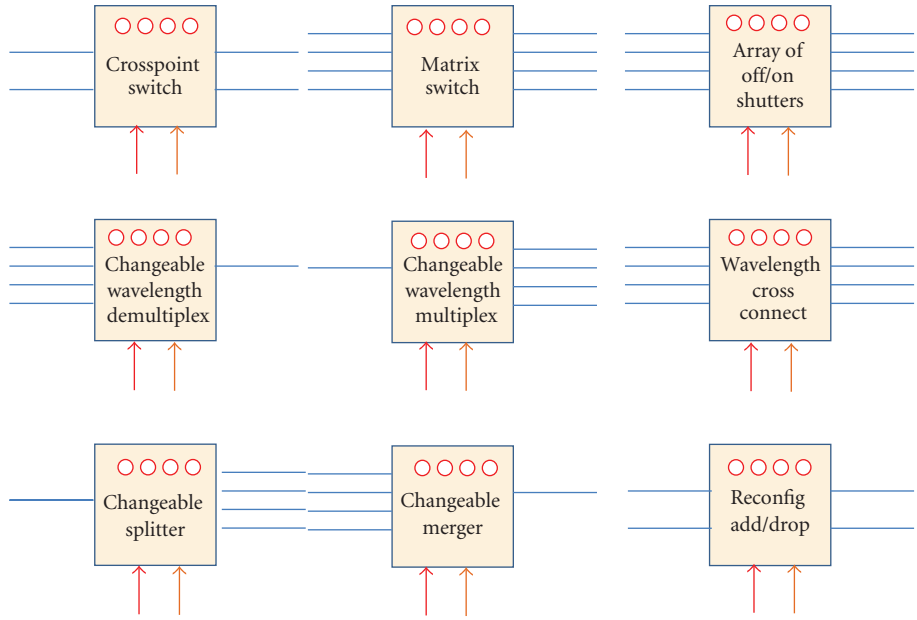


Figure 16: Programmable modules for reconfiguring the onchip optical waveguide paths (the interconnections).

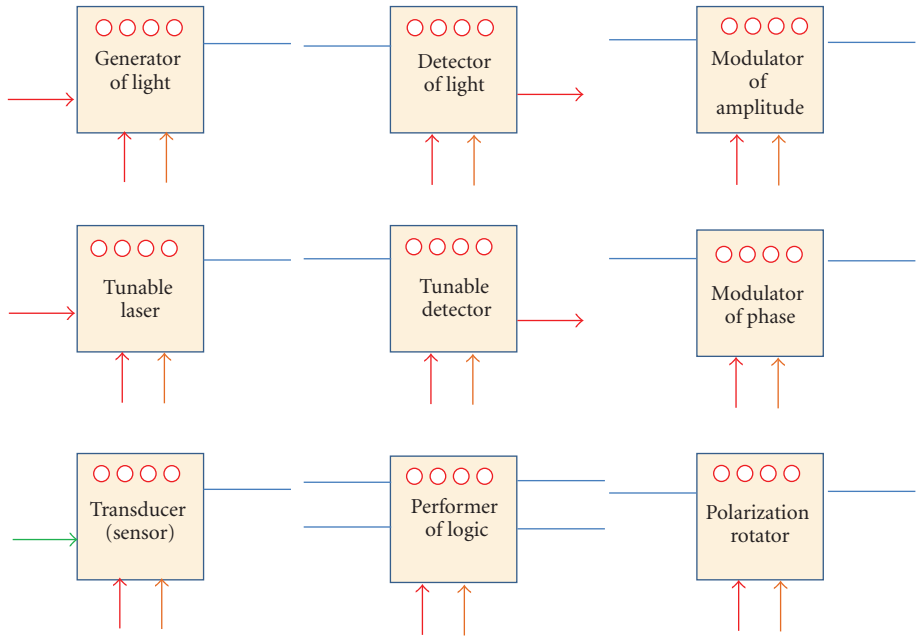


Figure 17: Dynamic programmable modules for generating, detecting, and modulating light (and for related functions).

and data mining. What are we describing specifically? Specifics are difficult to give because it is difficult to identify in advance the "killer applications" of the LSI chip. Nevertheless, let's go forward with some educated guesses. Some significant LSI functions are probably field-programmable optical gate arrays (optical logic for digital processing), optical memories-and-buffers, onchip spectrometers, microwave beam-steerers, agile RF/optical receivers, supercomputer optical routers, reconfigurable fiber-network nodes and intrachip communications in a multicore chip.

9. Examples of Actual RPIC Chips

The ongoing DARPA PHASER program targets a reconfigurable filter for agile microwave/photonic receivers in which optical lattice filters with adjustable poles and zeros are wanted. Teams working on this project have developed several excellent RPICs in both the InP-InGaAsP and silicon technologies. We've applied our theory to actual experiments by expressing their filter devices in terms of our modules. Figure 19 shows one stage (symbolically) of a lattice filter

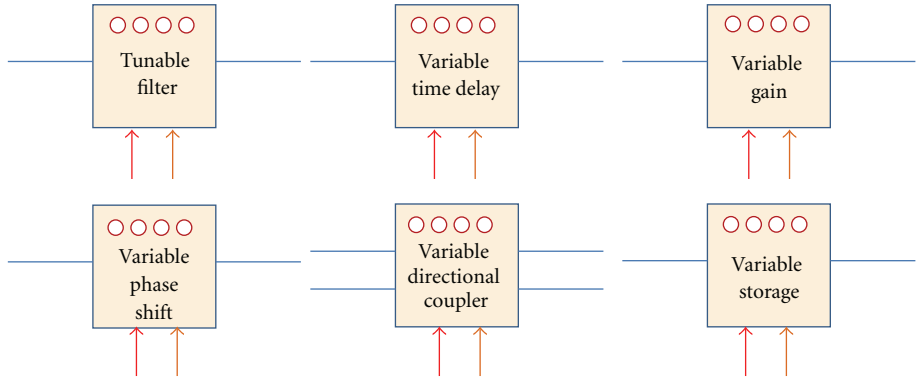


Figure 18: More dynamic modules.

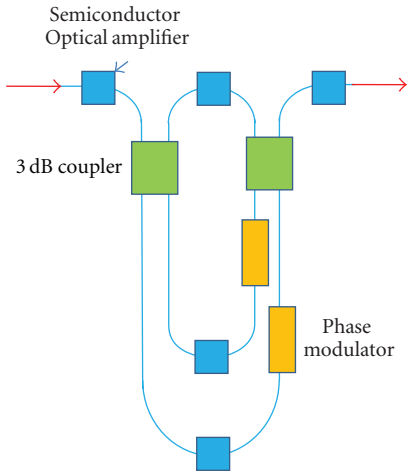


Figure 19: Building block expression of an actual [4] reconfigurable optical filter stage.

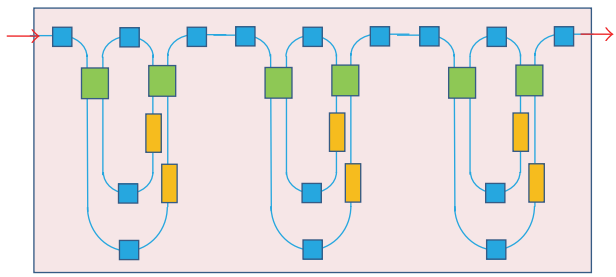


Figure 20: Three-stage lattice filter on chip. The color coding represents the Figure 19 modules.

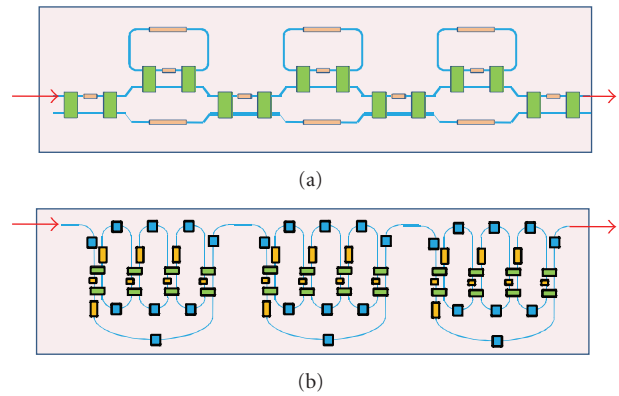
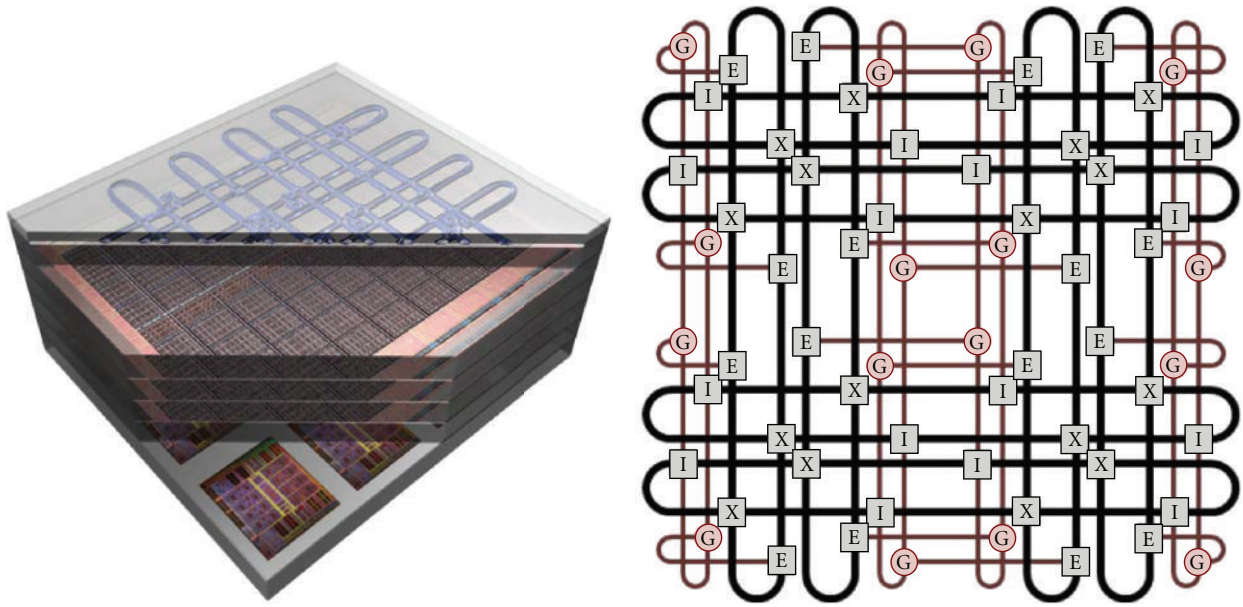


Figure 21: The onchip RPIC optical filters of: (a) Ibrahim [5] and (b) Guzzon [6] illustrated using the Figure 19 modules.

built by the UC Santa Barbara group [4]. That stage was then cascaded to make an experimental reconfigurable four-stage device on chip, three stages of which are shown in Figure 20. The same team created a more sophisticated lattice filter [6] as indicated in Figure 21(b). Silicon photonics technology was used by two teams [5, 16] with the UC Davis/Cornell group [5] constructing the filter of Figure 21(a). We find that our building blocks give an adequate representation of those real chip systems.

The modules of Figure 16 pertain to switching. In this context, there are compelling applications of RPIC optical routing in data centers via the high-speed large-scale switch-ona-chip. Such a switch has been built in InP technology [17] and the switch avoids O-E-O signal conversion. Another experimental chip is expressable via Figure 16: the bidirectional multiwavelength 4×4 electro-optical message router [18] developed by the Bergman group at Columbia University. This resonant microring-based device in silicon photonics technology is intended to be part of the photonic network-onchip (NoC) shown in Figure 22 where a scaleable broadcast network [19] links multiple cores in a computer chip.

Looking generally at optical interconnections, we can say that ROEICs have an excellent future as optical "nodes" or stations within fiber-optic WDM broadband access networks, content networks, enterprise networks and internet backbone networks. Nodes provide interconnections and local information exchange. In fact, there are already commercial products (Infinera) that perform this function. Researchers in the Bergman group have articulated a vision for optical network interface buffers in the CIAN initiative



(a) (b)

Figure 22: Bidirectional WDM switched optical network-onchip for intrachip communications as proposed by the Bergman group: (a) photonic layering on OE chip, (b) network topology.

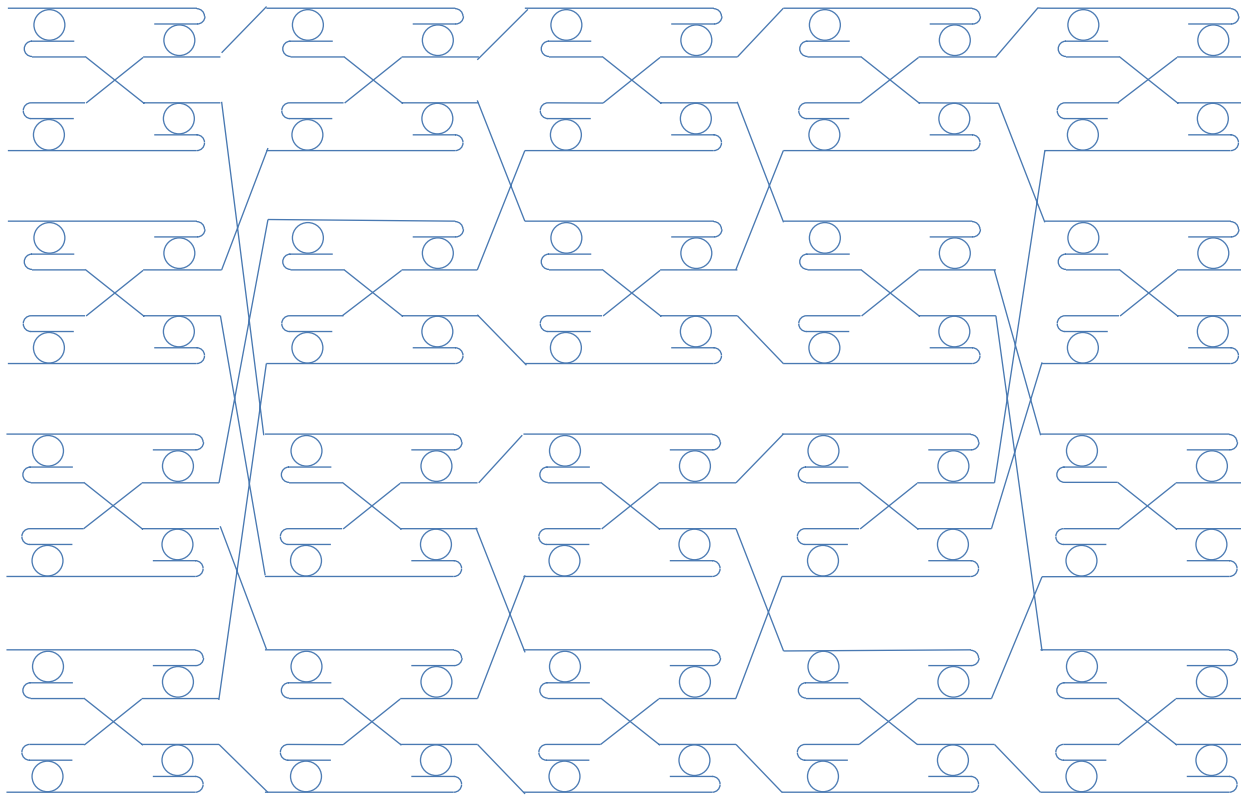


Figure 23: Reconfigurable 8×8 Benes optical matrix based upon [7].

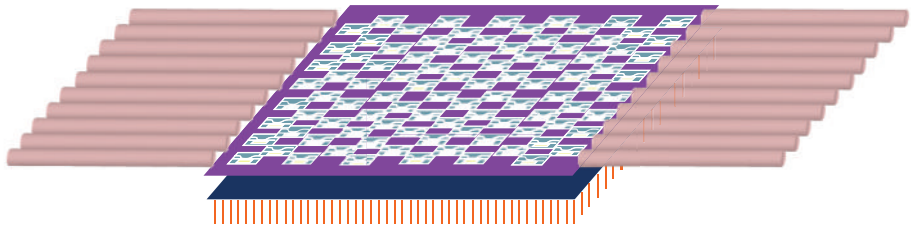


Figure 24: 256 × 256 matrix proposed for silicon photonics technology courtesy of Namiki [8].

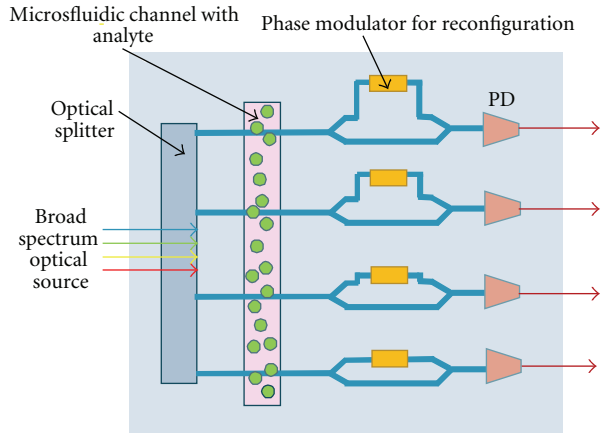


Figure 25: Primitive schematic of a reconfigurable finite-Fourier-transform spectrometer-ona-chip. The RPIC contains many more MZIs than those shown.

sponsored by NSF. The reconfigurable "optical substrate" [7] uses multiple stacked layers with cross-layer communications.

10. Proposed ROEICs and Reconfigurable OE Boards

In this section, we propose new ROEICs for future implementation. Turning again to Figure 16, we suggest reconfigurable large-scale optical matrices. Our first proposal is for a resonant 8 × 8 Benes-type optical router (Figure 23) based upon Figures 2(b) and 3(b) of Bianco et al. [20]. Each 2 × 2 module includes four EO microring resonators, two of which are reconfigured at a time. The next proposal comes from Shu Namiki [8] who suggested at a conference that a 256 × 256 matrix switch comprised of reconfigurable 2 × 2 MZI modules would helpful for data path selection in a data center [21]. Figure 24 is an artist's representation of that switch coupled to input and output fiber arrays. For the same digital path-processing application, Watts has proposed an innovative RPIC in WDM silicon photonics employing *pn* microdisk resonant devices [9].

An emerging photonic-sensor area is spectrometer-ona-chip [3] and here we propose in the Figure 25 top view an FTIR based upon the work of Florjańczyk et al. [22] and Okamoto [23]. The idea in Figure 25 is that the EO phase modulators (shown in orange) allow reconfiguration of the spectral range or resolution.

Our next proposal concerns optical computing. Over the past three decades, the approaches to optical computing have been partially successful at best. Nevertheless, the field is very much alive as evidenced by the 2008–2010 international conferences on "Optical Supercomputing" [24]. Practical solutions are coming closer. Digital optical logic on a chip is a frontier for this field and a reconfigurable logic "fabric" is an excellent direction for LSI ROEICs. Rather than sequential logic, the combinatorial "directed logic" (DL) approach of Hardy and Shamir [25] appears to be an effective way to implement the logic fabric. DL utilizes electro-optical waveguided elements and linear optics. We decided to add optical resonance (micro rings or disks) to DL so as to reduce dramatically the energy required to reconfigure the optical gate. The 2007 paper [25] shows circuits for AND/NAND, OR/NOR and XOR/XNOR. We propose in Figure 26 the resonant XOR/XNOR, cascadable among identicals. Unlike Zhang et al. [26], the Figure 26 unit cell features forward dropping of switched light and no waveguide crossovers.

An excellent physical embodiment of this DL gate would be the coupled *pn* microdisk device developed by Watts [9, 10], a 2 × 2 switch illustrated in Figure 27 (two such switches constitute Figure 26). He has optimized this carrier-depletion device so that only 10 fJ/bit is needed for switching each 2 × 2.

Recently a new type of DL has been invented [27]. It uses one 2 × 2 EO switch and one 1 × 1 EO switch per unit cell. Compared to the original form of DL, the new DL offers advantages in large-scale reconfigurable gate arrays, benefits

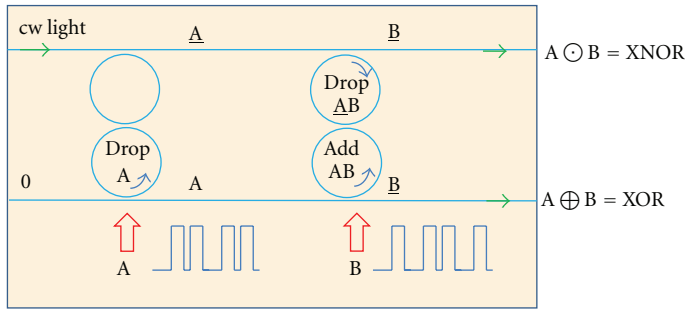


FIGURE 26: Optical directed-logic XOR/XNOR gate using two resonant 2×2 EO switches. Electrical logic signals A and B shift the resonators on and off of a resonance.

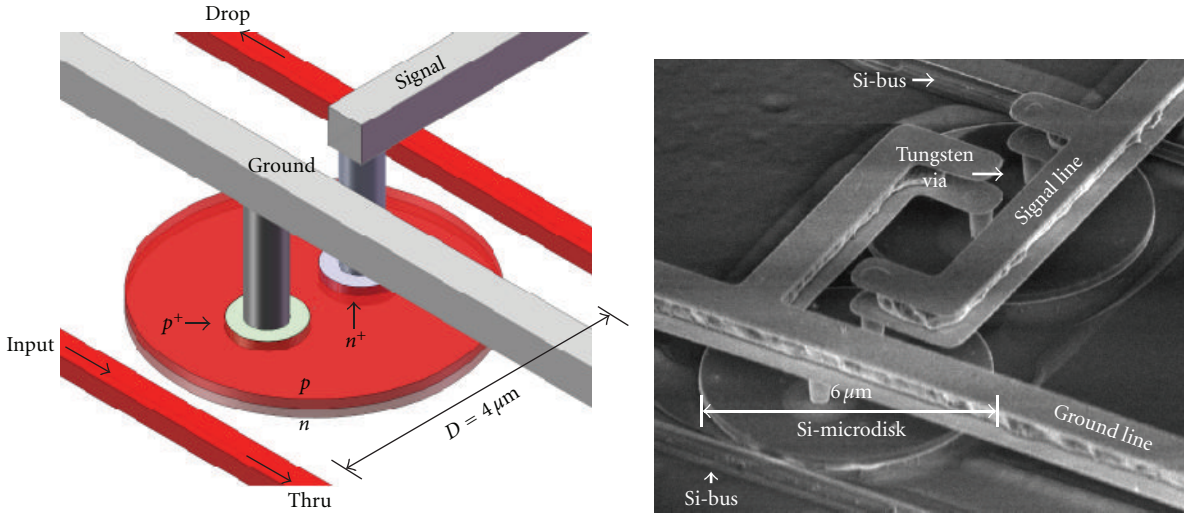


FIGURE 27: Proposed realization of a Figure 26 switch, courtesy of Michael Watts [9, 10].

such as lower latency and a smaller number of switches to perform the same overall logic function. The new DL can readily give N-bit adders and N-bit priority encoders. Arguably, the best hope for optical FGPAs resides in the new DL.

The development of quantum computers, especially optical quantum computers, is a futuristic activity; however, Jeremy O'Brien believes that the time horizon for OQC success can be brought closer in by using quantum walk correlation of two (or more) single-photon sources within a waveguided optical correlator PIC built upon a chip [28]. We share this vision of onchip optical quantum computing and to it we add a proposal of reconfigurablity in which the chip can provide different kinds of quantum computation.

Our final proposal is a reconfigurable optical controller for an $N \times M$ phased array microwave antenna. Our idea is to use a relatively small number of motherboards and reconfigurable chips: one board at a remote-control site is linked by a fiber bundle to the antenna plane where N boards are present. The overall system is a wavelength-multiplexed optical true-time delay RF beamsteerer for steering the beam in two dimensions. When the optical time delays are reconfigured in increments, the beam scans in steps of azimuth and elevation. In a schematic fashion, this system has already been designed by Riza and Madamopoulos as shown in Figure 9 of their paper [29]. With the help of Professor Riza, we have determined explicitly how to realize the system in SOI silicon photonics using AWG's, star couplers, EO switches, hybrid-integrated onchip laser diodes (LDs at each of N appropriate wavelengths), Ge photodiodes, onchip optical waveguide path delays, and off-chip dispersive fiber delay elements. The boards include, photonics as well as monolithically integrated microwave components such as transmit/receive switches, amplifiers and phase shifters. The resulting system is illustrated here in Figures 28, 29, 30, 31, 32, and 33. In all of these figures, the electrical control lines going to the active photonic components are not shown in order to keep the diagrams simple.

11. Conclusion

RPICs and ROEICs are going to play a major role in the future of the OE chip industry for both Si and InP. We have analyzed these ICs and have given a module theory

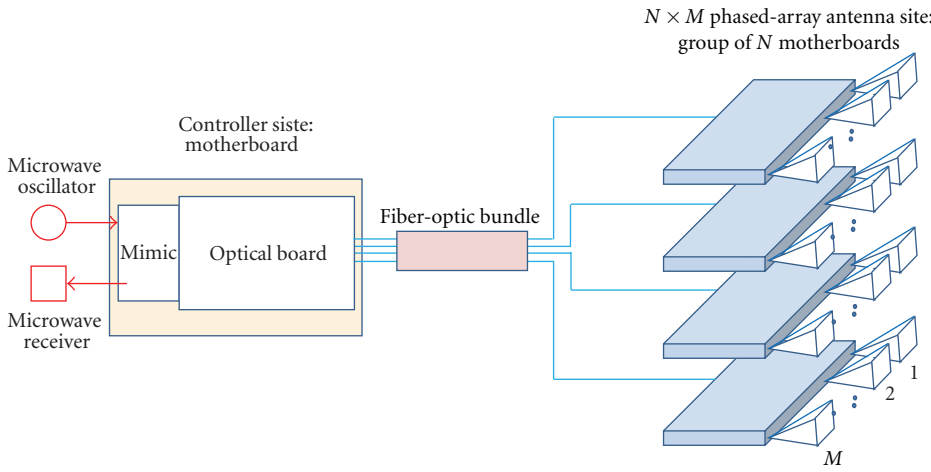


Figure 28: OE system-onboards for remote-controlled 2D beamsteering of a microwave phased-array antenna.

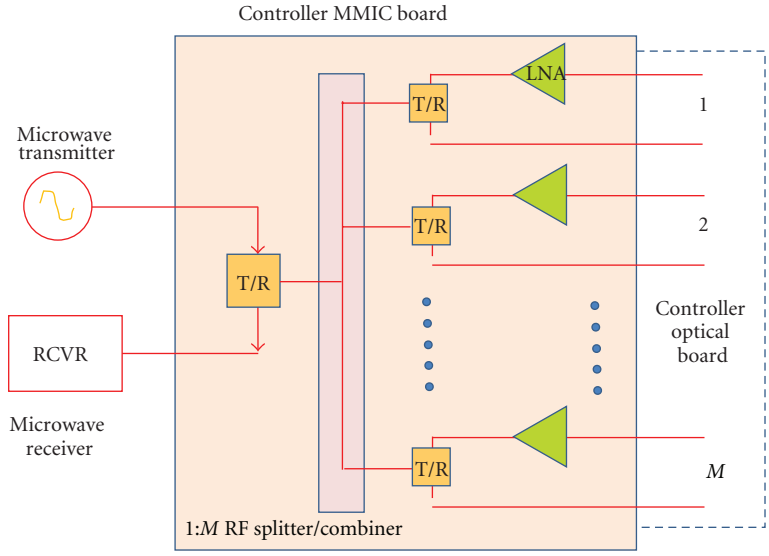


Figure 29: Close-up view of optical-MMIC board at the control site.

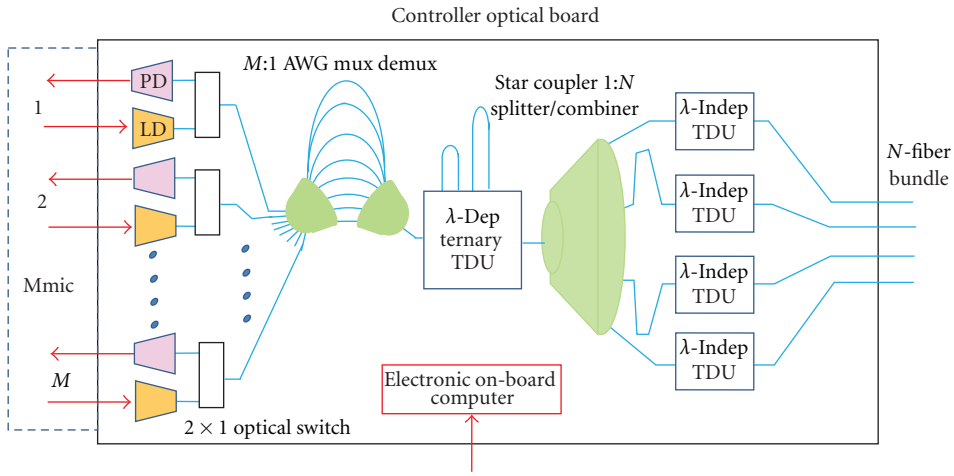


Figure 30: Close-up view of reconfigureable OE board at the control site.

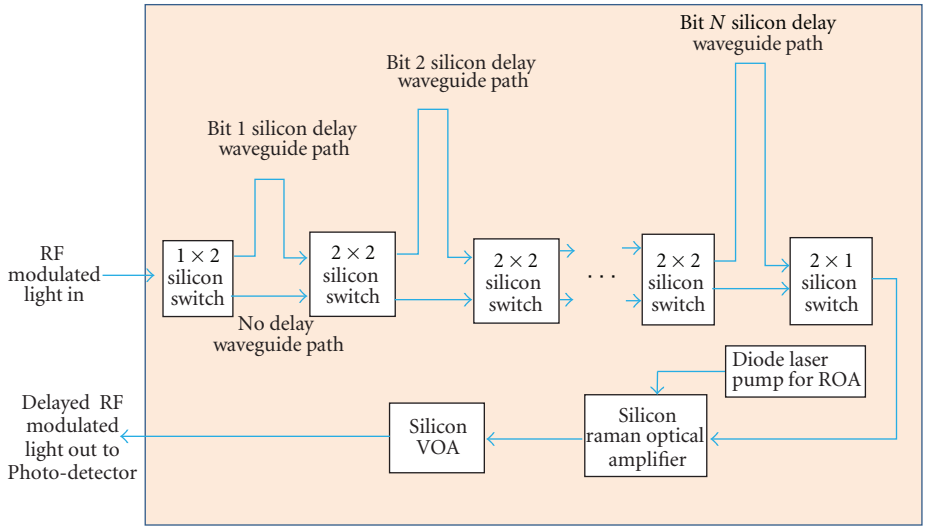


Figure 31: Wavelength-independent photonic time-delay unit in silicon with N-bit control [11].

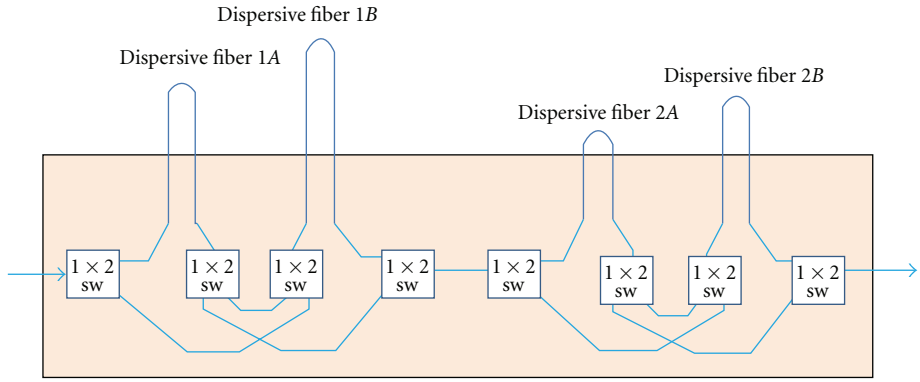


Figure 32: Wavelength-dependent photonic time-delay unit with two ternary-bit control.

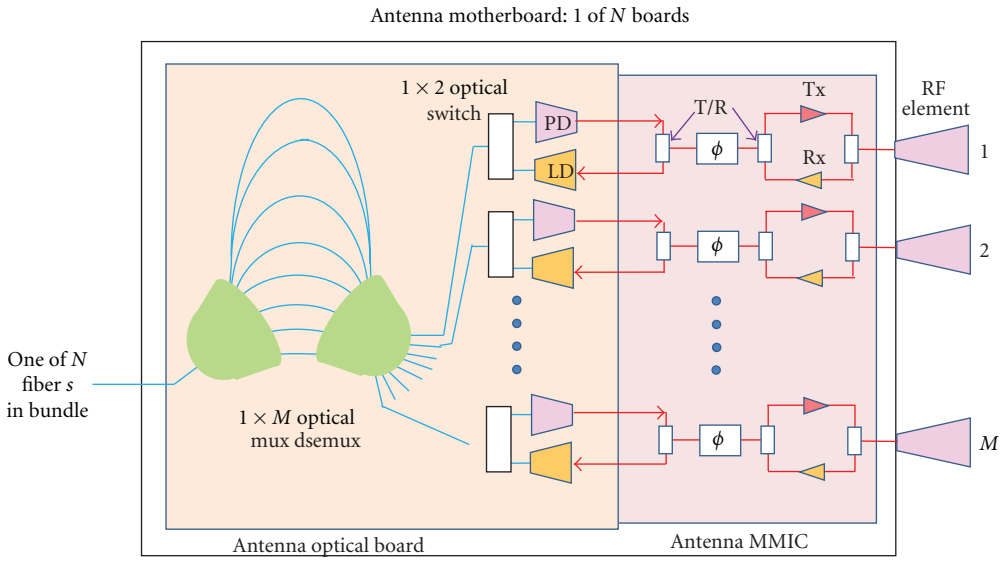


Figure 33: Optical/RF board situated at the antenna site (one board for each row).

for constructing "any" such chip using electro-optical components. New paradigms for 3D OE chips are suggested. We have examined the challenges of large-scale OE integration and have identified the principal reconfigurable-chip applications. Our block theory is applied here to lattice filters. In addition, new ROEICs are proposed in the areas of large-scale matrix switching, programmable optical-logic gate arrays in the directed-logic paradigm, and optically controlled beamsteering of a phased-array microwave antenna.

Acknowledgments

This work is supported by the Air Force Office of Scientific Research, Dr. Gernot Pomrenke, Program Manager. The author also wishes to thank Professor N. A. Riza for his collaboration on the RF beamformer.

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